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10/008,615	11/07/2001	William Edward Atherton	RPS920010104US1	3306

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EXAMINER	
ELMORE, REBA I	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,615	ATHERTON ET AL.	
	Examiner	Art Unit	
	Reba I. Elmore	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the c rrespondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☒ Claim(s) *1 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2002* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Pri rity under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/7/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-39 are presented for examination.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The abstract of the disclosure is objected to because acronyms must be defined when used in the abstract. Correction is required. See MPEP § 608.01(b).

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The disclosure is objected to because of the following informalities:

acronyms must be defined at their first usage in the disclosure;

'past' should be –passed—on page 17, line 9;

The use of the trademark 'Windows OS' and 'Microsoft Windows 2000' has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

Appropriate correction is required.

5. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

6. The claims are objected to because of the following informalities: claim 1, line 12 and claim 19, line 14 both have the term 'block' misspelled.

Appropriate correction is required.

35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakagawa.

9. Nakagawa teaches the invention (claim 1) as claimed including a system for directing memory allocation in a data processing system, the system comprising:

means, responsive to a request for allocation of memory by an application executing on the data processing system, for allocating a block of memory to the application (e.g., see col. 5, line 43 to col. 6, line 15);

means for translating a virtual address of the memory block allocated into its corresponding physical address within memory the virtual address being equivalent to logical addresses associated with the physical pages of the first and second storage (e.g., see col. 8, lines 6-26);

means for querying the physical address to determine if it is a physical address desired by the application, wherein the desired physical address is specified by the application and provided as parameter value to components carrying out the memory allocation devices (e.g., see Figures 3-4); and,

means for passing the memory block for utilization by the application only when the physical address matches the desired physical address (e.g., see col. 8, line 43 to col. 9, line 12).

As to claim 2, Nakagawa teaches the invention as further comprising:

means, responsive to the memory block allocated not having the desired physical address as the linking and mapping of the program elements to the memory elements (e.g., see Figure 5);

allocating another block of memory to the application (e.g., see Figure 5); and,

repeating the translating and querying steps for the another block of memory, wherein the allocating and repeating steps are completed until the memory blocks allocated include the desired physical address (e.g., see Figure 5).

As to claim 3, Nakagawa teaches the means for allocating memory comprises means for concurrently locking down memory blocks allocated to prevent repetitive allocation of the memory blocks as part of the copy-on write memory management process (e.g., see Figure 20).

As to claim 4, Nakagawa teaches the memory block allocated includes all of the desired physical address, for de-allocating portions of the memory block allocated that to not contain the desired physical address as maintaining and controlling the in-use list (e.g., see Figure 6).

As to claim 5, Nakagawa teaches the desired physical address comprises a range of memory addresses that is at least as large as a size of memory required by the application within the range of memory addresses, the system further comprising means for prompting a user to enter parameter values for the range of memory addresses and the size of memory (e.g., see col. 10, line 47 to col. 11, line 35).

As to claim 6, Nakagawa teaches the data processing system is a multi-node system having a first and a second processing system each with individual memory wherein, the allocating means allocates a memory block on a memory of the second processing system for an application executing on the first processing system and the translating means translates the virtual address to a physical address on the memory of the second processing system (e.g., see col. 10, line 47 to col. 11, line 35).

As to claim 7, Nakagawa teaches the allocating means initially allocates all of the available memory to the application and the comparing means includes immediately de-allocating portions of the allocated memory not with the range (e.g., see col. 12, lines 37-62).

As to claim 8, Nakagawa teaches a means for selecting an algorithm for completing the allocation and repeating steps, wherein the algorithm is selected from among several available algorithms based on an indication by a user, wherein further, absent the indication, a default algorithm is automatically selected (e.g., see col. 8, lines 27-42).

As to claim 9, Nakagawa teaches the selecting means differentiates among several calculation processes for determining a maximum amount of memory to allocate during each allocating step, the calculation processes including:

(1) calculating the maximum amount of memory to allocate as an amount of physical memory in the system as maintaining the control tables (e.g., see Figures 3-5);

(2) calculating the maximum amount of memory to allocate as the result of (amount of physical memory in the system – size of the range requested) + the amount of physical memory required as maintaining the control tables for the first and second storage devices as well as the physical and logical space (e.g., see Figures 1-5);

(3) calculating the maximum amount of memory to allocate as an amount of available physical memory in the system as maintaining the control tables (e.g., see Figures 3-5); and,

(4) calculating the maximum amount of memory to allocate as the result of (amount of available physical memory in the system – size of the range requested) + the amount of memory required by the application, wherein the range is a range of addresses comprising the desired physical address and one of the calculation processes is utilized as maintaining the control tables as well as the management data storing area (e.g., see Figures 3-5).

As to claim 10, Nakagawa teaches the allocating means includes means for allocating the memory block in a chunk size, which is gradually reduced as more memory with the desired physical address is allocated (e.g., see col. 8, lines 5-25).

As to claim 11, Nakagawa teaches the invention further comprising:

means for organizing allocated blocks of memory into address order (e.g., see Figure 4);

means for determining a section of the allocated blocks with the desired physical address that has maximum continuity (e.g., see Figure 4); and,

means for passing the section to the application, wherein when the section is not as large as a memory space required, additional sections with the desired physical address are allocated and passed, wherein a memory space required is an actual size of physical memory required by the application and a size of the desired physical address is at least as large as the memory space required (e.g., see Figure 4).

As to claim 12, Nakagawa teaches determining means comprises means for moving a size X window over the allocated blocks, wherein X is the amount of memory space required by the application (e.g., see Figures 4-5).

As to claim 13, Nakagawa teaches means for organizing the allocated memory in a pattern similar to a pattern provided by a Window's operating system and the querying means includes means for conducting a search for a match to the pattern provided by the Window's operating system (e.g., see Figures 4-5).

As to claim 14, Nakagawa teaches the data processing system comprises a cache with a cache size of Z units, wherein the system includes means for providing a separation of Z units between allocated memory pages to enable tracking of cache misses (e.g., see Figures 4-5).

10. Nakagawa teaches the invention (claim 15) as claimed including a method for allocating memory on a data processing system comprising:

receiving a specific physical memory location to allocate to processes of an application (e.g., see Figure 4);

executing the application on the data processing system, wherein the application requires access to memory of the data processing system (e.g., see Figure 4); and,

responsive to an operation requesting access to memory by the application, automatically assigning the specific physical memory location to the operation (e.g., see Figure 4).

As to claim 16, Nakagawa teaches:

calculating a physical memory location corresponding to a virtual address provided by the operation (e.g., see Figure 5);

interactively allocating memory blocks and comparing a physical address of the allocated memory blocks with the specific physical memory location, wherein, when the allocated memory block is within the physical memory location the allocated memory block is passed to the application (e.g., see Figure 5).

As to claim 17, Nakagawa teaches the allocated memory block comprising all required memory within the specific physical memory location, de-allocating all allocated memory block not within the specific physical memory location as maintaining and controlling the in-use list (e.g., see Figure 6).

11. Nakagawa teaches the invention (claim 19) as claimed including a computer program product for directing memory allocation in a data processing system, the program product comprising:

a computer readable medium (e.g., see Figures 3-5);

program instructions on the computer readable medium for:

responsive to a request for allocation of memory by an application executing on the data processing system, allocating a block of memory to the application (e.g., see Figures 3-5);

translating a virtual address of the memory block allocated into its corresponding physical address within memory (e.g., see Figures 3-5);

querying the physical address to determine if it is a physical address desired by the application, wherein the physical address desired is specified by the application and provided as a parameter value to components carrying out the memory allocation (e.g., see Figures 3-5); and,

passing the memory block for utilization by the application only when the physical address matches the desired physical address (e.g., see Figures 3-5).

As to claim 20, Nakagawa teaches program instructions for:

responsive to the memory block allocated not having the desired physical address (e.g., see Figures 3-5);

allocating another block of memory to the application (e.g., see Figures 3-5); and,

repeating the translating and querying steps for the another block of memory, wherein the allocating and repeating steps are completed until the memory blocks allocated include the desired physical address (e.g., see Figures 3-5).

As to claim 21, Nakagawa teaches the program instructions for allocating of memory further comprising program instructions for concurrently locking down memory blocks allocated to prevent repetitive allocation of the memory blocks as part of the copy-on write memory management process (e.g., see Figure 20).

As to claim 22, Nakagawa teaches program instructions for when the memory block allocated includes all of the desired physical address, de-allocating portions of the memory block allocated that do not contain the desired physical address as maintaining and controlling the in-use list (e.g., see Figure 6).

As to claim 23, Nakagawa teaches the desired physical address comprises a range of memory address that is at least as large as a size of memory required by the application within the range of memory addresses, the program product further comprising program instructions for prompting a user to enter parameter values for the range of memory addresses and the size of memory prior to execution of the application (e.g., see col. 8, lines 8-42).

As to claim 24, Nakagawa teaches the data processing system is multi-node system having a first and a second processing system each with individual memory, wherein:

the allocating program instructions allocates a memory block on a memory of the second processing system for an application executing on the first processing system (e.g., see Figures 2-4) and,

the translating program instructions translates the virtual address to a physical address on the memory of the second processing system (e.g., see col. 5, line 55 to col. 6, line 31).

As to claim 25, Nakagawa teaches the computer program product, wherein:

the program instructions for allocating initially allocates all of the available memory to the application (e.g., see Figures 3-4) and,

wherein the program instructions for comparing includes instructions for immediately de-allocating portions of the allocated memory not within the range (e.g., see Figures 3-4).

As to claim 26, Nakagawa teaches the program instructions for selecting an algorithm for completing the allocating and repeating steps, wherein the algorithm is selected from among several available algorithms based on an indication by a user, wherein further, absent the indication, a default algorithm is automatically selected (e.g., see Figure 6).

As to claim 27, Nakagawa teaches the program instructions for selecting an algorithm includes instructions for differentiating among several calculation processes for determining a maximum amount of memory to allocate during each allocating step, the calculation processes including:

(1) calculating the maximum amount of memory to allocate as an amount of physical memory in the system as maintaining the control tables (e.g., see Figures 3-5);

(2) calculating the maximum amount of memory to allocate as the result of (amount of physical memory in the system – size of the range requested) + the amount of physical memory required as maintaining the control tables for the first and second storage devices as well as the physical and logical space (e.g., see Figures 1-5);

(3) calculating the maximum amount of memory to allocate as an amount of available physical memory in the system (e.g., see Figures 3-5); and,

(4) calculating the maximum amount of memory to allocate as the result of (amount of available physical memory in the system – size of the range requested) + the amount of memory required by the application, wherein the range is a range of addresses comprising the desired physical address and one of the calculation processes is utilized as maintaining the control tables as well as the management data storing area (e.g., see Figures 3-5).

As to claim 28, Nakagawa teaches the program instructions for allocating the memory includes instructions for allocating the memory block in a chunk size, which is gradually reduced as more memory with the desired physical address is allocated (e.g., see Figures 3-5).

As to claim 29, Nakagawa teaches the algorithm comprises a window function, wherein the program instructions further comprises instructions for checking the allocated memory in blocks and sliding the window across the blocks to determine whether the blocks fit within the window, wherein the window includes a start address and an end address within the desired physical address (e.g., see Figures 3-5).

As to claim 30, Nakagawa teaches program instructions for:

organizing allocated blocks of memory into address order (e.g., see Figure 4);

determining a section of the allocated blocks within the desired physical address that has maximum continuity (e.g., see Figure 4); and,

passing the section to the application, wherein when the section is not as large as a memory space required, additional sections with the desired physical address are allocated and passed, wherein a memory space required is an actual size of physical memory required by the application and a size of the desired physical address is at least as large as the memory space required (e.g., see Figure 4).

As to claim 31, Nakagawa teaches the program instructions for determining a section comprises instructions for moving a size X window over the allocated blocks, wherein X is the amount of memory space required by the application (e.g., see Figures 4-5).

As to claim 32, Nakagawa teaches program instructions for:

organizing the allocated memory in a pattern similar to a pattern provided by a Window's operation system (e.g., see col. 1, line 11 to col. 4, line 5); and,

conducting a search for a match to the pattern provided by the Window's operation system (e.g., see col. 1, line 11 to col. 4, line 5).

As to claim 33, Nakagawa teaches the data processing system comprises a cache with a cache size of Z units, wherein the method includes providing a separation of Z units between allocated memory pages to enable tracking of cache misses (e.g., see Figure 4).

12. Nakagawa teaches the invention (claim 34) as claimed including a data processing system comprising:

a processor that executes application processes (e.g., see Figure 3);

a memory interconnect to the processor (e.g., see Figure 3);

an operating system (e.g., see col. 1, lines 17-30); and,

means for allocating pre-selected, specific physical memory locations to the application processes (e.g., see Figures 3-4).

As to claim 35, Nakagawa teaches the means comprising:

means for receiving a specific physical memory location to allocate to processes of an application (e.g., see Figures 3-4);

means for executing the application on the data processing system, wherein the application requires access to memory of the data processing system (e.g., see Figures 3-4); and,

means, responsive to an operation requesting access to memory by the application, for automatically assigning the specific physical memory location to the operation (e.g., see Figures 3-4).

As to claim 36, Nakagawa teaches the system further comprising:

means for calculating a physical memory location corresponding to a virtual address provided by the operation (e.g., see col. 7, lines 32-54); and,

means for interactively allocating memory blocks and comparing a physical address of the allocated memory blocks with the specific physical memory location, wherein, when the allocated memory block is within the physical memory location the allocated memory block is passed to the application (e.g., see Figures 3-4).

As to claim 37, Nakagawa teaches the means, responsive to some of the allocated memory block comprising all the required memory within the specific memory location, for de-allocating all allocated memory block not within the specific physical memory location as maintaining and controlling the in-use list (e.g., see Figure 6).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on M-TH from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2187, Donald Sparks, can be reached for general questions concerning this application at (571) 272-4201. Additionally, the official fax phone number for the art unit is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2187

December 11, 2004